

PATENT

POWER TRANSISTOR STRUCTURE
WITH NON-UNIFORM METAL WIDTHS

BRIEF DESCRIPTION OF THE DRAWINGS

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FIGs. 1A-1C are a series of plan views illustrating an example of a power transistor structure 100 in accordance with the present invention.

FIGs. 2A-2N are a series of cross-sectional diagrams illustrating an example of a method of forming a transistor structure in accordance 10 with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGs. 1A-1C show a series of plan views that illustrate an example 15 of a power transistor structure 100 in accordance with the present invention. As described in greater detail below, structure 100 provides a more even current density, thereby reducing the source-to-drain turn on resistance, by using metal lines with non-uniform widths.

As shown in FIG. 1A, power transistor structure 100, which is 20 formed in a p-type semiconductor material 110, such as a well, includes a number of n+ strips 112 that are formed in semiconductor material 110. The n+ strips 112, in turn, include alternating drain strips 112A and source 112B strips.

As further shown in the FIG. 1A, power transistor structure 100 25 also includes a gate structure 114 that is formed over, and insulated from, semiconductor material 110. Gate structure 114 includes a number of gate strips 114A that are formed between the n+ strips 112, and a gate connector 114B that is connected to an end of each of the gate strips 114A.

In addition, power transistor structure 100 includes a number of p+ strips 116 that are formed in semiconductor material 110. In the FIG. 1A example, two horizontal p+ strips 116 and a vertical p+ strip 116 are shown where the vertical p+ strip 116 contacts an end of the 5 horizontal p+ strips 116.

As shown in FIG. 1B, power transistor structure 100 further includes an interconnect structure 120 that is formed over semiconductor material 110. Interconnect structure 120, in turn, includes a number of contacts 122 that are connected to the n+ strips 10 112, the gate connector 114B, and the p+ strips 116.

Interconnect structure 120 also includes a number of metal-1 strips 124 that are formed over, and insulated from, semiconductor material 110. The metal-1 strips 124, in turn, include alternating metal drain strips 124A that are connected to the contacts 122 which are 15 connected to the n+ drain strips 112A, and metal-1 source strips 124B that are connected to the contacts 122 which are connected to the n+ source strips 112B.

In addition, interconnect structure 120 includes a metal-1 strip 126 that is formed over, and insulated from, semiconductor material 20 110. The metal-1 strip 126 is connected to the contacts 122 which are connected to the gate connector 114B. Interconnect structure 120 further includes a number of metal-1 strips 130 that are formed over, and insulated from, semiconductor material 110. The metal-1 strips 130 are connected to the contacts 122 which are connected to the p+ strips 25 116.

As shown in FIG. 1C, interconnect structure 120 further includes a number of vias 132 that are connected to the metal-1 drain and source strips 124A and 124B. As additionally shown in FIG. 1C, power

transistor structure 100 includes a metal structure 134 that is formed over interconnect structure 120.

Metal structure 134, in turn, includes alternating metal-2 drain strips 134A that are connected to the vias 132 which are connected to 5 the metal-1 drain strips 124A, and metal-2 source strips 134B that are connected to the vias 132 which are connected to the metal-1 source strips 124B. In addition, metal structure 134 includes a drain connector 136A that is connected to an end of each drain strip 134A, and a source connector 136B that is connected to an end of each source strip 136B.

10 In accordance with the present invention, the metal-2 drain strips 134A have widths WA that are non-uniform. In the example shown in FIGs. 1A-1C, the metal-2 drain strips 134A include a center metal-2 strip 140 and outer metal-2 strips 142 where the widths WA of the metal-2 drain strips 134A increase from the center metal-2 strip 140 to the outer 15 metal-2 strips 142.

Similarly, the metal-2 source strips 134B have widths WB that are non-uniform. In the example shown in FIGs. 1A-1C, the metal-2 source strips 134B include a center metal-2 strip 144 and outer metal-2 strips 146 where the widths WB of the metal-2 source strips 134B increase 20 from the center metal-2 strip 144 to the outer metal-2 strips 146. In addition, center metal-2 strip 140 and center metal-2 strip 144 have equal widths, although non-equal widths can also be used.

One of the advantages of using metal-2 drain and source strips with non-uniform widths is that the widths of the metal-2 drain and 25 source strips can be sized to reduce variations in current density across the structure. This, in turn, reduces the source-to-drain turn on resistance and maximizes the overall current carrying capacity of power transistor structure 100.

If the variation in current density across a power transistor structure is large, then the areas that carry a higher current density are more prone to overheating or hot electron degradation, and hence provide the limit for safe operation. As a result, by reducing variations 5 in the current density across the power transistor structure, the overall current carrying capacity of power transistor structure can be increased.

Although the example shown in FIGs. 1A-1C shows metal-2 drain and source strips that increasingly get wider as the drain and source strips move towards the periphery, other combinations can also be used 10 depending on the variations in current density of the power transistor structure.

For example, the metal-2 strips can get increasingly narrower as the strips move towards the periphery. In addition, the metal-2 strips can be formed in groups where each group includes a number of metal- 15 2 strips. In this case, one group of metal-2 strips can have a first width, while another group of metal-2 strips can have a second different width. Further, although the present invention has been illustrated with metal-2 strips, metal strips formed from other metal layers can also be used.

FIGs. 2A-2N show a series of cross-sectional diagrams that 20 illustrate an example of a method of forming a power transistor structure in accordance with the present invention. As shown in FIG. 2A, the method, which utilizes a p-well 210 that is formed in an n-well 212 which, in turn, is formed in a p-type substrate 214, begins by forming a layer of gate oxide 220 on p-well 210. Alternately, p-well 210 25 can be directly formed in a p-type substrate. (Conventional steps can be used to set the threshold voltage of the to-be-formed transistor structure.)

After gate oxide layer 220 has been formed, a layer of polysilicon 222 is formed on gate oxide layer 220. Next, a gate mask 224 is formed

and patterned on polysilicon layer 222. Following this, as shown in FIG. 2B, the exposed regions of polysilicon layer 222 are etched to form a gate structure that includes a number of spaced-apart polysilicon gate strips 226, and a gate connector that is connected to an end of each of 5 the gate strips 226. Once the etch is complete, gate mask 224 is removed.

Next, as shown in FIG. 2C, an implant mask 230 is formed and patterned on p-well 210 to expose the gate structure and adjacent regions of p-well 210. Following this, an n-type dopant, such as 10 phosphorous, is implanted into p-well 210 and the gate structure to form a number of n+ strips 232 and dope the gate structure, including the gate strips 226 and the gate connector. The n+ strips 232, in turn, include alternating drain strips 232A and source 232B strips. Once the implant is complete, implant mask 230 is removed.

15 As shown in FIG. 2D, after implant mask 230 has been removed, an implant mask 234 is formed and patterned on p-well 210 to protect the gate structure and the n+ strips 232. Following this, a p-type dopant, such as boron, is implanted into p-well 210 to form a number of connected p+ strips 236. Once the implant is complete, implant mask 20 234 is removed.

FIG. 1A shows the structure that results following the removal of mask 234, where FIG. 2D is taken along lines 2D-2D of FIG. 1A, n+ strips 232 represent n+ strips 112, the gate structure with gate strips 226 and the gate connector represents gate structure 114 with gate 25 strips 114A and gate connector 114B, and the p+ strips 236 represent p+ strips 116.

As shown in FIG. 2E, after implant mask 234 has been removed, a layer of isolation material 240 is formed on gate oxide layer 220 and the gate structure. Once formed, isolation layer 240 is planarized using

conventional methods. Following this, a contact mask 242 is formed and patterned on isolation layer 240 to expose regions on the top surface of isolation layer 240 that lie over the n+ strips 232, the p+ strips 236, and a portion of the gate structure.

5 Following this, as shown in FIG. 2F, the exposed regions of isolation layer 240 and the underlying layer of gate oxide 220 are then etched to form contact openings 244 that expose regions on the surfaces of the n+ strips 232, the p+ strips 236, and a portion of the gate structure. Once the etch is complete, contact mask 242 is

10 removed.

Once contact mask 242 has been removed, a layer of contact metal is formed on isolation layer 240 to fill up the contact openings 244. (A diffusion barrier can be formed on the exposed n+ and p+ strips using conventional methods. In addition, contact openings to the 15 gate structure can be formed in a separate set of masking and etching steps.)

As shown in FIG. 2G, after the layer of contact metal has been formed, the layer of contact metal is planarized using conventional methods to remove the layer of contact metal from the top surface of 20 isolation layer 240. The planarization step forms contacts 246 in the contact openings 244 that make electrical connections with the n+ drain and source strips 232A and 232B, the p+ strips 236, and the gate connector of the gate structure.

After this, as shown in FIG. 2H, a layer of metal-1 250 is formed 25 on isolation layer 240 and the contacts 246 to make electrical connections with the contacts 246. Next, a metal-1 mask 252 is formed and patterned on metal-1 layer 250. As shown in FIG. 2I, the exposed regions of metal-1 layer 250 are etched until the exposed regions of

metal-1 layer 250 have been removed from the top surface of isolation layer 240.

As further shown in FIG. 2I, the etch forms alternating metal-1 drain strips 254A, which are connected to the contacts 246 that are 5 connected to the n+ drain strips 232A, and metal-1 source strips 254B, which are connected to the contacts 246 that are connected to the n+ source strips 232B.

The etch also forms a metal-1 gate strip that is connected to the contacts 246 which are connected to the gate connector of the gate 10 structure, and metal-1 strips 256 that are connected to the contacts 246 which are connected to the p+ strips 236. Once the etch is complete, metal-1 mask 252 is removed.

FIG. 1B shows the structure that results following the removal of mask 252, where FIG. 2I is taken along lines 2I-2I of FIG. 1B, contacts 15 246 represent contacts 122, metal-1 drain and source strips 254A and 254B represent metal-1 drain and source strips 124A and 124B, the metal-1 gate strip represents metal-1 gate strip 126, and metal-1 strips 256 represent metal-1 strips 130.

As shown in FIG. 2J, after metal-1 mask 252 has been removed, 20 a layer of isolation material 260 is formed on isolation layer 240, metal-1 strips 254A and 254B, metal-1 strips 256, and the metal-1 gate strip formed over, and electrically connected to, the gate connector of the gate structure.

Once isolation layer 260 has been formed, isolation layer 260 is 25 planarized using conventional methods. Following this, a via mask 262 is formed and patterned on isolation layer 260 to expose regions on the top surface of isolation layer 260 that lie over the metal-1 drain and source strips 254A and 254B.

Following this, as shown in FIG. 2K, the exposed regions of isolation layer 260 are then etched to form via openings 264 that expose regions on the surfaces of the metal-1 drain and source strips 254A and 254B. Once the etch is complete, via mask 262 is removed. Next, a 5 layer of via metal is formed on isolation layer 260 to fill up the contact openings 264.

As shown in FIG. 2L, after the layer of via metal has been formed, the layer of via metal is planarized using conventional methods to remove the layer of via metal from the top surface of isolation layer 10 260. The planarization step forms vias 266 in the contact openings 264 that make electrical connections with the metal-1 drain and source strips 254A and 254B.

After this, as shown in FIG. 2M, a layer of metal-2 270 is formed on isolation layer 260 and the vias 266 to make electrical connections 15 with the vias 266. Next, a metal-2 mask 272 is formed and patterned on metal-2 layer 270. As shown in FIG. 2N, the exposed regions of metal-2 layer 270 are then etched until the exposed regions of metal-2 layer 270 have been removed from the top surface of isolation layer 260.

20 As further shown in FIG. 2N, the etch forms a drain structure with spaced-apart metal-2 drain strips 274 and a drain connector that is connected to an end of each drain strip 274. The metal-2 drain strips, in turn, are connected to the vias 266 that are connected to the metal-1 drain strips 254A.

25 The etch also forms a source structure with spaced-apart metal-2 source strips, and a source connector that is connected to an end of each source strip. The source strips, in turn, are connected to the vias 266 that are connected to the metal-1 source strips 254B. Once the

etch is complete, metal-2 mask 272 is removed. Following this, the method continues with conventional back end processing steps.

FIG. 1C shows the structure that results following the removal of mask 272, where FIG. 2N is taken along lines 2N-2N of FIG. 1C, the vias 266 represent the vias 132, the metal-2 drain strips 274 represent the metal-2 drain strips 134A, the metal-2 drain connector represents the metal-2 drain connector 136A, the metal-2 source strips represent the metal-2 source strips 134B, and the metal-2 source connector represents the metal-2 source connector 136B.

It should be understood that the above descriptions are examples of the present invention, and that various alternatives of the invention described herein may be employed in practicing the invention. Thus, it is intended that the following claims define the scope of the invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.